# Numerical Simulation of GaAs MESFET's with a p-Buffer Layer on the Semi-Insulating Substrate Compensated by Deep Traps

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*Abstract*—**Numerical simulation of GaAs MESFET's with a p-buffer layer on the semi-insulating substrate is performed in which impurity compensation by traps in the substrate is considered. It is shown that the use of a thicker p-buffer layer results in lower device current due to the formation of a steeper barrier at the channel–substrate interface. It is also shown that in a case with higher acceptor and trap densities in the substrate, the drain current becomes lower due to the decrease in the substrate current. This decrease in the substrate current occurs due to the formation of a negative space-charge layer in the substrate. It is concluded that using a thick p-buffer layer has the same effect as using a substrate with a high density of traps inasmuch as both of them lead to minimizing the short-channel effects in GaAs MESFET's.**

## I. INTRODUCTION

GaAs MESFET's fabricated on semi-insulating GaAs substrates are now very important devices for realizing high-speed integrated circuits and monolithic microwave integrated circuits (MMIC's). The semi-insulating substrate provides a good isolation between devices in IC's and minimizes the parasitic capacitances. Some problems, however, arise from the fact that the substrate is "semi-insulating." It is well known that MESFET characteristics strongly depend on junction properties between an n-type active layer and the substrate [1]–[3]. This is because the semi-insulating material property is achieved by impurity compensation by traps [4] and hence a space-charge layer is formed at the active layer–substrate interface [5]. The increase in substrate current with increasing drain voltage is believed to be an important cause for the short-channel effects, and so a device structure with a buried p-layer is proposed [6]. The high performance of this structure has been reported [7], [8].

Computer-aided analysis is now a very useful technology in optimizing the design of semiconductor devices. Several numerical works for GaAs MESFET's have been reported [9]–[16]. However, most of the models neglect the impurity compensation by traps in the substrate, which strongly affects the device characteristics, as mentioned above. To take account of the potential barrier at the active layer–substrate interface, some authors treated a case with a p-type (buffer) layer as a substrate [11], [13], [15]. But, only a few numerical works have included effects of deep levels in the semi-insulating substrate [14], [16]. Therefore, the performance of GaAs MESFET's with a p-buffer layer on the semi-insulating substrate has not yet been accurately estimated.

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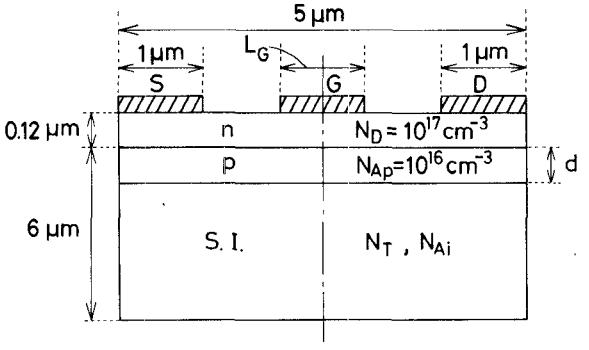


Fig. 1. Schematic diagram of a modeled GaAs MESFET with a p-buffer layer on the semi-insulating substrate.

In a previous paper [17], we briefly reported some calculated results on GaAs MESFET's with a p-buffer layer on the substrate including deep traps. In this work, we have systematically simulated GaAs MESFET's with a p-buffer layer on the semi-insulating substrate, in which impurity compensation by deep traps is considered. We describe the model first. Next, calculated results are described with emphasis placed on the effects of using a p-buffer layer on the MESFET's characteristics. Effects of the impurity compensation by traps on the MESFET's characteristics are also described. It is finally shown that using a thick p-buffer layer has the same effect as using a substrate with a high density of traps inasmuch as both of them lead to minimizing the short-channel effects in GaAs MESFET's.

## II. MODEL

### A. Device Structure

The device structure simulated in this study is shown in Fig. 1. The donor density in the active layer of the MESFET, $N_D$, is $10^{17}\,cm^{-3}$, and its thickness is 0.12 $\mu$m, so that it can be a normally off or slightly normally on

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type. The acceptor density in the p-buffer layer, $N_{Ap}$, is set to be $10^{16}\,\mathrm{cm}^{-3}$. As a semi-insulating substrate, we assume an undoped semi-insulating LEC (liquid encapsulated Czochralski) GaAs, where deep donors "EL2" compensate shallow acceptors [18]. In this case, ionized deep donors act as electron traps [5]. The gate length, $L_G$, and the thickness of the p-buffer layer, $d$, are varied, as parameters, to study the MESFET's characteristics. The deep donor density, $N_T$, and the shallow acceptor density, $N_{Ai}$, in the substrate are typically set to be $5\times10^{14}\,\mathrm{cm}^{-3}$ and $5\times10^{13}\,\mathrm{cm}^{-3}$, respectively [17]. But, in some cases, they are also varied as parameters while keeping $N_{Ai}/N_T = 0.1$, which corresponds to an equilibrium electron density of $10^{7}\,\mathrm{cm}^{-3}$ in the substrate.

### B. Basic Equations and Material Parameters

In general, the basic equations for device analysis become rather complex when deep levels are included [16]. In the present case, however, a simplified approach is adopted. We treat the steady-state condition and, further, neglect the contribution from holes because the trap "EL2" is an electron trap [5], [16]. The neglect of holes can actually be justified when the p-buffer layer is fully depleted. Thus the basic equations become the following.

a) Poisson's equation:

$$\nabla^2\psi = -\frac{q}{\epsilon}(-n + N_D - N_A + N_T^+) \tag{1}$$

$$N_T^+ = \frac{N_C \exp\{-(E_C - E_T)/kT\}}{n + N_C \exp\{-(E_C - E_T)/kT\}} N_T. \tag{2}$$

b) Continuity equation of electron current:

$$\nabla \cdot \boldsymbol{J}_n = 0. \tag{3}$$

c) Electron current equation

$$\boldsymbol{J}_n = -q\mu_n n \nabla\psi + qD_n \nabla n. \tag{4}$$

The meanings of the symbols are as follows:

- $\psi$ Electrostatic potential.
- $q$ Electron charge.
- $\epsilon$ Dielectric permittivity.
- $n$ Electron density.
- $N_D$ Shallow donor density.
- $N_A$ Shallow acceptor density.
- $N_T^+$ Ionized deep donor density.
- $N_C$ Effective density of states in the conduction band.
- $E_C$ Energy level of the bottom of the conduction band.
- $E_T$ Energy level of the deep donor "EL2."
- $k$ Boltzmann's constant.
- $T$ Absolute temperature.
- $\boldsymbol{J}_n$ Electron current density.
- $\mu_n$ Electron mobility.
- $D_n$ Electron diffusion coefficient.

The trap energy level $E_T$ and the transport coefficients $\mu_n$ and $D_n$ should be given to solve the above equations. Here $E_C - E_T$ is assumed to be 0.69 eV at $T = 300$ K [4]. The Einstein relation is assumed to hold between the mobility and the diffusion coefficient, and the field dependence of the mobility is taken into account as given below:

$$\mu_n = \mu_{n0}\frac{1 + (v_{ns}/\mu_{n0}|E|)(E/E_0)^4}{1 + (E/E_0)^4} \tag{5}$$

where $E$ is the electric field. $E_0 = 4000$ V/cm and $v_{ns} = 8.5\times10^6$ cm/s; $\mu_{n0}$ is the low-field electron mobility and is assumed in this study to be 4500 $\mathrm{cm}^2$/Vs both in the n layer ($10^{17}\,\mathrm{cm}^{-3}$) and in the semi-insulating substrate.

### C. Discretization and Boundary Conditions

The basic equations are put into discrete forms by the finite difference method. The Scharfetter–Gummel formulation is adopted for the discretization of the current equation [19].

As boundary conditions, equilibrium electron densities are assumed at the source and drain contacts. At these contacts, electrostatic potentials are set equal to the applied voltages. At the gate contact, a barrier height of 0.8 eV is assumed, and the electron density is determined based on the thermionic emission theory. At free surfaces, the normal derivatives of current density and electrostatic potential are set to zero; that is, an ideal surface is assumed, as has usually been done.

The discretized equations are solved by an iterative method based on Gummel's scheme [20].

## III. Results and Discussions

### A. Device Characteristics

We have calculated the drain current–drain voltage ($I_D$–$V_D$) characteristics and the drain current–gate voltage ($I_D$–$V_G$) characteristics of GaAs MESFET's with gate lengths of 0.3 $\mu$m, 0.5 $\mu$m, 1 $\mu$m, and 2 $\mu$m. The thickness of the p-buffer layer, $d$, is varied from 0 to 0.3 $\mu$m. The shallow acceptor density, $N_{Ai}$, and the deep donor density, $N_T$, in the substrate are $5\times10^{13}\,\mathrm{cm}^{-3}$ and $5\times10^{14}\,\mathrm{cm}^{-3}$, respectively. Note that in the two-level compensation model considered here, $N_{Ai}$ is equal to the density of empty traps in the substrate under equilibrium [5]. It should also be noted that when $d \leqslant 0.3$ $\mu$m, the p-buffer layer is fully depleted and a neutral p-region does not exist. We have confirmed, by the full two-carrier simulation, that the current–voltage characteristics shown below are the same as those calculated by taking into account the contribution from holes.

Fig. 2 and Fig. 3 show calculated examples of $I_D$–$V_D$ characteristics of 0.3-$\mu$m- and 2-$\mu$m-gate-length MESFET's, respectively. In these figures, (a) is for a MESFET on the semi-insulating substrate without a p-buffer layer, and (b) and (c) are for MESFET's with a p-buffer layer on the semi-insulating substrate. From these, we can point out the following features.

1) Without a p-buffer layer, the drain currents increase more rapidly with drain voltage, particularly for a shorter gate length MESFET. The transconductance

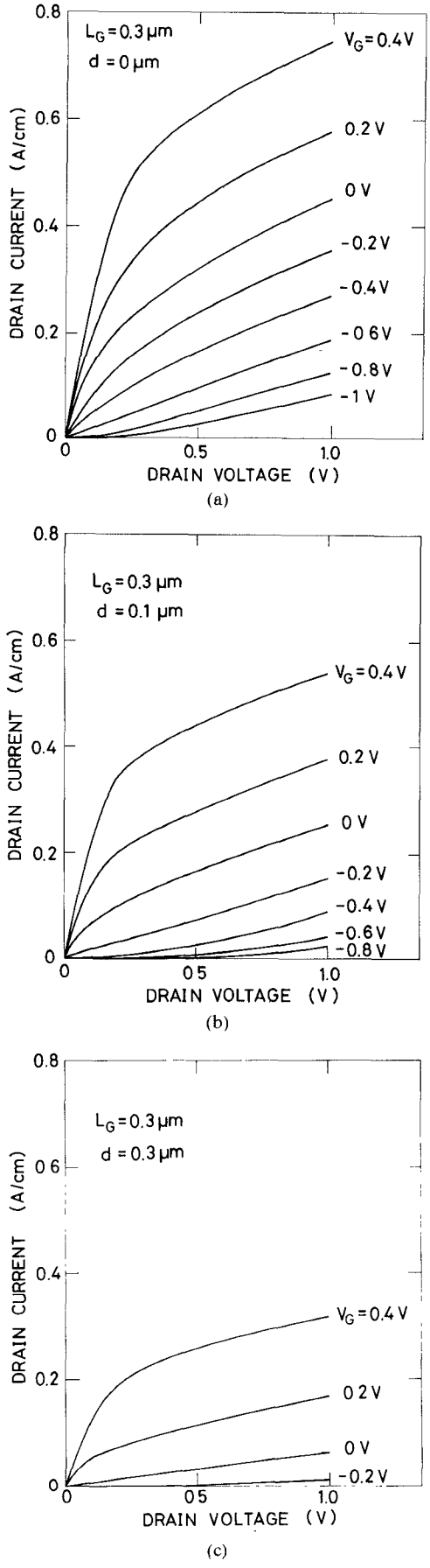


Fig. 2 Calculated drain current–drain voltage characteristics of 0.3-μm-gate-length GaAs MESFET's with a p-buffer layer thickness of $d$. (a) $d = 0$ μm; (b) $d = 0.1$ μm; (c) $d = 0.3$ μm. The shallow acceptor density $N_{A}$, and the deep donor density $N_T$ in the substrate are $5\times10^{13}$ cm$^{-3}$ and $5\times10^{14}$ cm$^{-3}$, respectively.

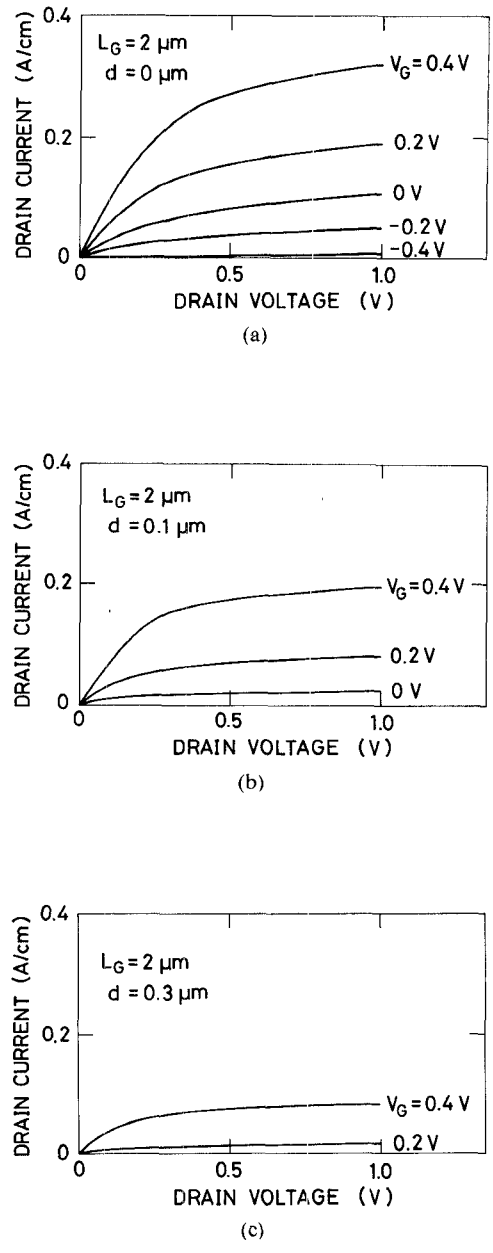


Fig. 3. Calculated drain current–drain voltage characteristics of 2-μm-gate-length GaAs MESFET's with a p-buffer layer thickness of $d$. (a) $d = 0$ μm; (b) $d = 0.1$ μm; (c) $d = 0.3$ μm. The shallow acceptor density $N_{A}$, and the deep donor density $N_T$ in the substrate are $5\times10^{13}$ cm$^{-3}$ and $5\times10^{14}$ cm$^{-3}$, respectively.

is lower in a relatively low current region ($\leqslant 0.2$ A/cm).

2) The drain current is lower in the case with a thicker p-buffer layer.

The nonsaturation of drain currents can be explained by the presence of current conduction through the substrate. This substrate current flows directly from the n-layer at the source side to the drain through the substrate, and is noticeable in the case with lower acceptor density in the substrate [5], [16]. Therefore, the contribution of substrate conduction is most pronounced, as seen in Fig. 2 and Fig. 3, for a shorter gate length MESFET without a p-buffer layer. The presence of substrate conduction means that

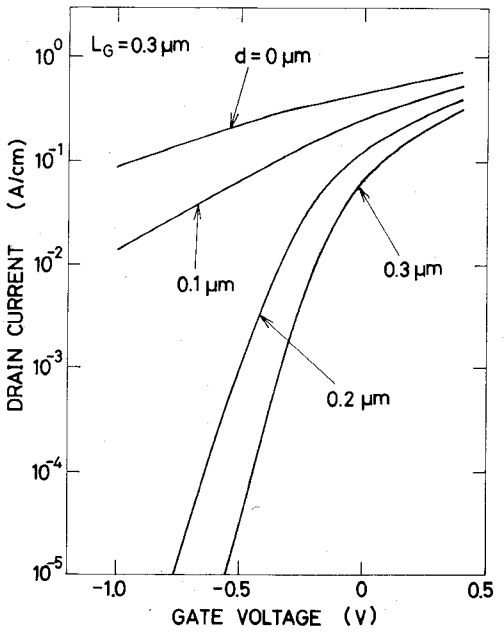


Fig. 4. Drain current–gate voltage characteristics of 0.3-$\mu$m-gate-length GaAs MESFET's, with the thickness of a p-buffer layer $d$ as a parameter. $N_{Ai} = 5\times10^{13}$ cm$^{-3}$ and $N_T = 5\times10^{14}$ cm$^{-3}$. $V_D = 1$ V.

current flows far from the gate, resulting in a lower transconductance in the region where the substrate current is dominant.

Next, we discuss the dependence of device characteristics on the thickness of the p-buffer layer. Fig. 4 shows the calculated $I_D$–$V_G$ characteristics of 0.3-$\mu$m-gate-length MESFET's as a function of the thickness $d$ of the p-buffer layer. As mentioned before, the drain current is lower in the case with a thicker p-buffer layer. This can be understood by considering the formation of a space-charge layer at the active layer–substrate interface. Fig. 5 and Fig. 6 show the potential profiles and the current distributions, respectively, for different thicknesses of the p-buffer layer. It is understood that for thicker $d$, the barrier at the active layer–substrate interface is steeper due to the higher density of negative charges in the substrate. This opposes electron injection into the substrate, leading to a decrease in the contribution of substrate current, as seen in Fig. 6. In addition to this effect, the negative charges in the substrate must be compensated by positively ionized donors in the active layer. So the channel becomes effectively thinner by this space-charge effect, and the drain current becomes smaller for a thicker p-buffer layer. The drain current reduction by this space-charge effect is observed for relatively low $V_D$ ( $< 0.2$ V), where the substrate current is not dominant.

As shown above, the MESFET's characteristics are strongly influenced by the presence of a p-buffer layer. The use of a thick p-buffer layer reduces the contribution of substrate conduction. It is speculated that even if the trap density in the substrate is low and the contribution of substrate current is significant, it can be reduced by introducing a p-buffer layer or a buried p-layer.

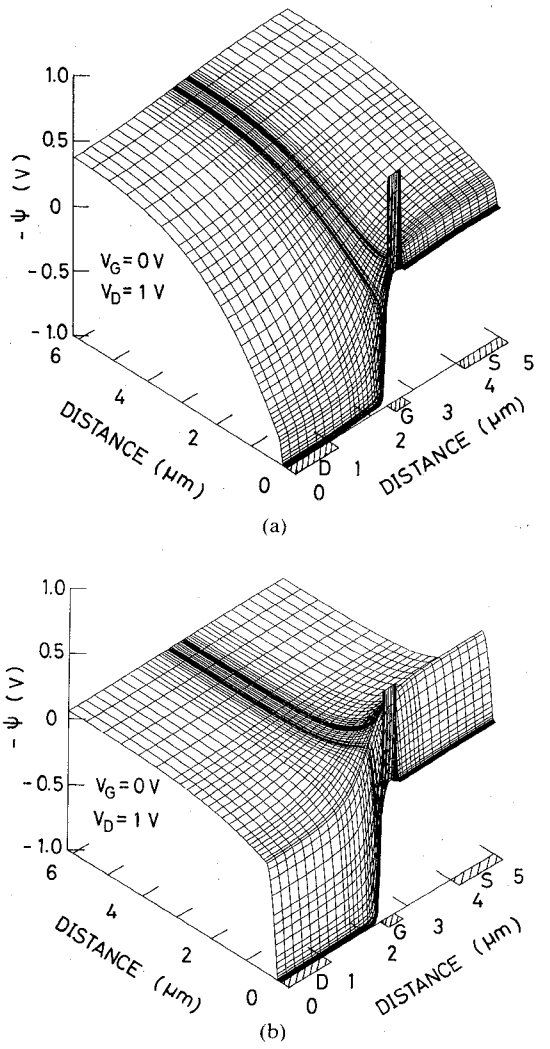


Fig. 5. Comparison of potential profiles of 0.3-$\mu$m-gate-length GaAs MESFET's with different p-buffer layer thickness $d$. $N_{Ai} = 5\times10^{13}$ cm$^{-3}$ and $N_T = 5\times10^{14}$ cm$^{-3}$. $V_D = 1$ V and $V_G = 0$ V. (a) $d = 0.1$ $\mu$m. (b) $d = 0.3$ $\mu$m.

### B. Effects of Impurity Compensation in the Substrate

In the previous section, the trap density, $N_T$, and the acceptor density, $N_{Ai}$, in the substrate are set to be $5\times10^{14}$ cm$^{-3}$ and $5\times10^{13}$ cm$^{-3}$, respectively. In this section, to study the effects of impurity compensation in the substrate, we have calculated the $I_D$–$V_D$ characteristics and $I_D$–$V_G$ characteristics of GaAs MESFET's with a p-buffer layer on the semi-insulating substrate in which $N_T$ and $N_{Ai}$ are varied while keeping $N_{Ai}/N_T = 0.1$. This corresponds to an equilibrium electron density of $10^7$ cm$^{-3}$ in the substrate.

Fig. 7(a) and (b) shows the calculated $I_D$–$V_D$ characteristics of 0.3-$\mu$m-gate-length GaAs MESFET's with different trap and acceptor densities in the substrate. These are for MESFET's without a p-buffer layer. It is seen that for higher $N_T$ and $N_{Ai}$ in the substrate, the drain currents are lower and their increases with drain voltage are less noticeable. These effects can be explained by the fact that for higher $N_{Ai}$, the barrier at the active layer–substrate interface is steeper due to a higher density of negative charges

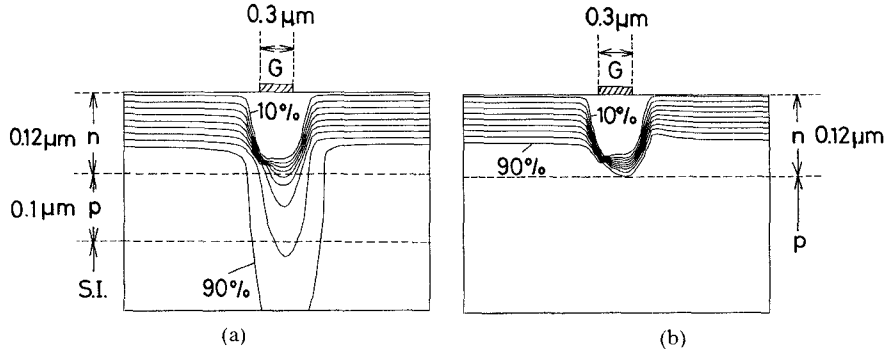


Fig. 6. Comparison of current distributions of 0.3-$\mu$m-gate-length GaAs MESFET's with different p-buffer layer thickness $d$. $N_{Ai}=5\times10^{13}$ cm$^{-3}$ and $N_T=5\times10^{14}$ cm$^{-3}$. $V_D=1$ V and $V_G=0$ V. (a) $d=0.1$ $\mu$m (b) $d=0.3$ $\mu$m.

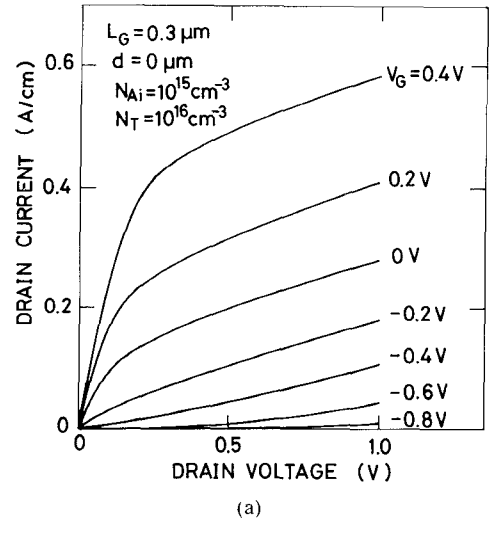


Fig. 7. Calculated drain current–drain voltage characteristics of 0.3-$\mu$m-gate-length GaAs MESFET's without a p-buffer layer ($d=0$ $\mu$m) The trap and acceptor densities in the substrate are higher than those in Fig. 2(a). (a) $N_{Ai}=10^{15}$ cm$^{-3}$, $N_T=10^{16}$ cm$^{-3}$ (b) $N_{Ai}=10^{16}$ cm$^{-3}$, $N_T=10^{17}$ cm$^{-3}$.

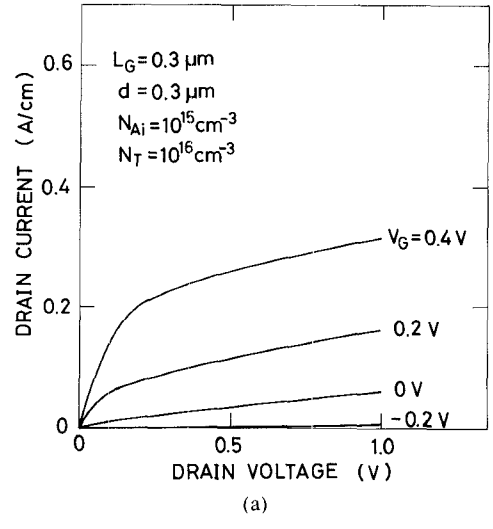


Fig. 8. Calculated drain current–drain voltage characteristics of 0.3-$\mu$m-gate-length GaAs MESFET's with a p-buffer layer thickness $d$ of 0.3 $\mu$m. The trap and acceptor densities in the substrate are higher than those in Fig. 2(c). (a) $N_{Ai}=10^{15}$ cm$^{-3}$, $N_T=10^{16}$ cm$^{-3}$. (b) $N_{Ai}=10^{16}$ cm$^{-3}$, $N_T=10^{17}$ cm$^{-3}$.

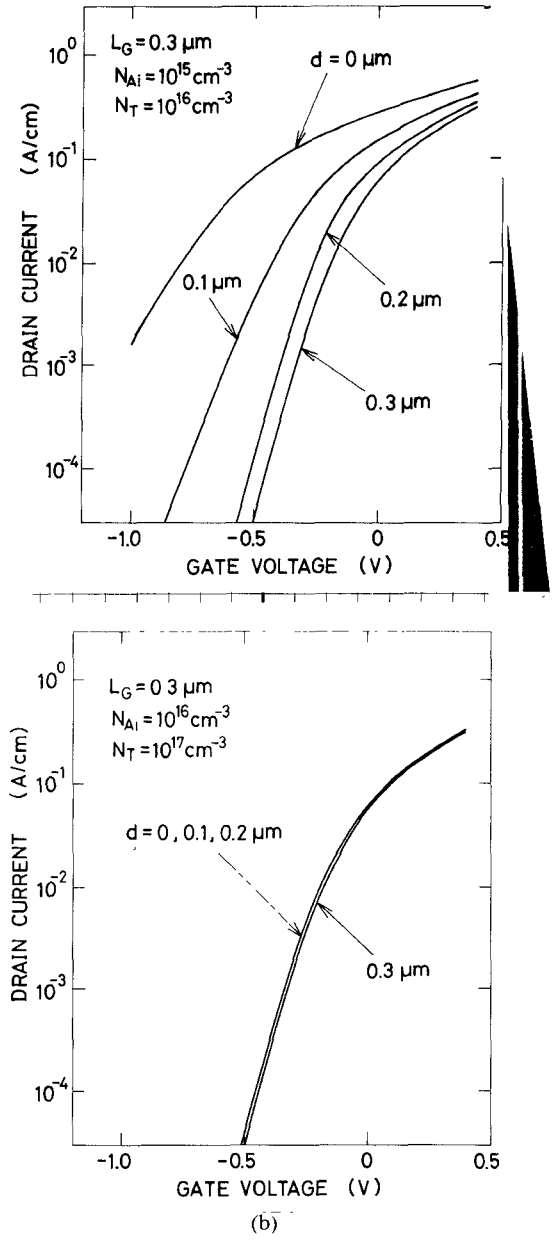


Fig. 9. Drain current–gate voltage characteristics of 0.3-$\mu$m-gate-length GaAs MESFET's, with the thickness of a p-buffer layer, $d$, as a parameter. The trap and acceptor densities in the substrate are higher than those in Fig. 4. $V_D = 1$ V. (a) $N_{Ai} = 10^{15}$ cm$^{-3}$, $N_T = 10^{16}$ cm$^{-3}$. (b) $N_{Ai} = 10^{16}$ cm$^{-3}$, $N_T = 10^{17}$ cm$^{-3}$.

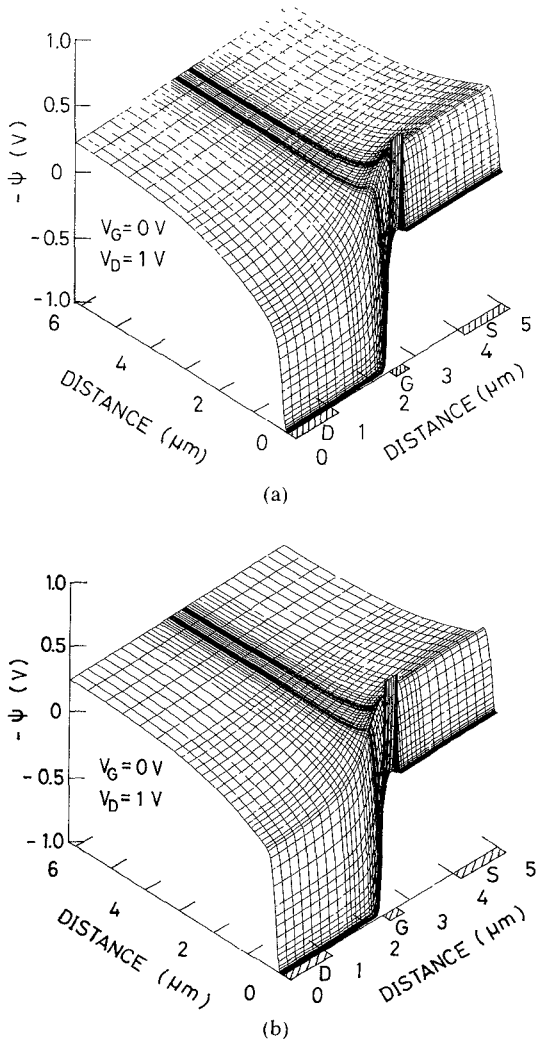


Fig. 10. Potential profiles of 0.3-$\mu$m-gate-length GaAs MESFET's (a) without a p-buffer layer and (b) with a p-buffer layer thickness of 0.3 $\mu$m. $N_{Ai} = 10^{16}$ cm$^{-3}$ and $N_T = 10^{17}$ cm$^{-3}$, $V_D = 1$ V and $V_G = 0$ V. Note that $N_{Ai} = N_{Ap}$ in this case

in the substrate. This opposes electron injection into the substrate, leading to the decrease in the substrate current. To give another physical explanation, $N_{Ai}$ is, in the two-level compensation model considered here, equal to the density of empty traps under equilibrium, and so the thickness of the trap-filled region in the substrate under equilibrium (which is equal to $(2\epsilon V_B/qN_{Ai})^{1/2}$, where $V_B$ is the built-in potential at the n–i junction [5]) becomes thinner for higher $N_{Ai}$, leading to the lower substrate current.

Fig. 8(a) and (b) shows the calculated $I_D$–$V_D$ characteristics of 0.3-$\mu$m-gate-length GaAs MESFET's with a p-buffer layer thickness of 0.3 $\mu$m. The impurity densities in the substrate are the same as those used in Fig. 7(a) and (b), respectively. They are similar to the $I_D$–$V_D$ curves shown in Fig. 7(b), where the acceptor and trap densities in the substrate are higher than those in Fig. 7(a) and the substrate current is lower. These results suggest that the use of a thick p-buffer layer has the same effect as using a substrate with high density of traps in the sense that both of them reduce the substrate current.

Fig. 9 shows the calculated $I_D$–$V_G$ characteristics of 0.3-$\mu$m-gate-length GaAs MESFET's, with the thickness of the p-buffer layer, $d$, as a parameter. Two cases with different trap and acceptor densities in the substrate are shown. As in the case shown in Fig. 4, the drain currents are lower for a thicker p-buffer layer when $N_T$ and $N_{Ai}$ are relatively low (Fig. 9(a)). However, in the case of $N_{Ai} = 10^{16}$ cm$^{-3}$ and $N_T = 10^{17}$ cm$^{-3}$ (Fig. 9(b)), there is little dependence of $I_D$–$V_G$ curves on $d$. This is because in this case $N_{Ai} = N_{Ap}$ and so, as is shown in Fig. 10, the potential distributions at the active layer–substrate interface show little dependence on the thickness of the p-buffer layer if it is fully depleted. It should be noted that in the case of

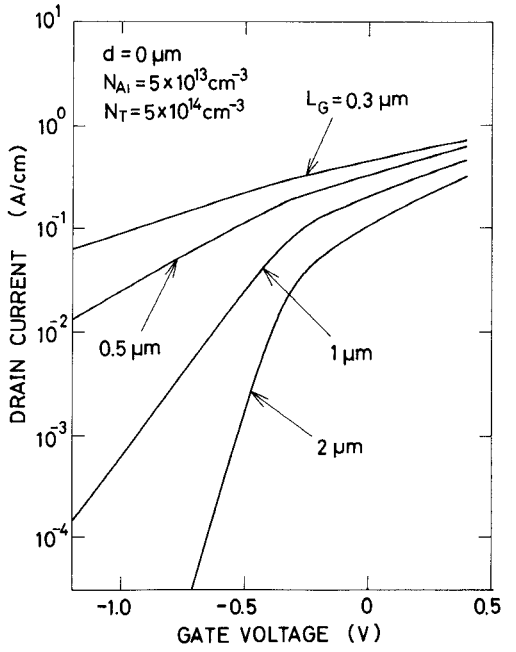


Fig. 11. Gate length dependence of $I_D$–$V_G$ characteristics of GaAs MESFET's on a compensated substrate ($N_{A_i} = 5\times10^{13}$ cm$^{-3}$, $N_T = 5\times10^{14}$ cm$^{-3}$) without a p-buffer layer.

$d = 0.3$ μm, the $I_D$–$V_G$ curves are, as seen in Fig. 4 and Fig. 9, almost the same as for the case without a p-buffer layer ($d = 0$ μm) and with high acceptor and trap densities in the substrate ($N_{A_i} = 10^{16}$ cm$^{-3}$, $N_T = 10^{17}$ cm$^{-3}$). This can be understood from the fact that in the case of $N_{A_i} = 10^{16}$ cm$^{-3}$ in the substrate (with $d = 0$ μm), the thickness of the trap-filled region or the space-charge region in the substrate under equilibrium, which is given by $(2\epsilon V_B/qN_{A_i})^{1/2}$, is 0.293 μm and is comparable to the thickness of the p-buffer layer (0.3 μm) considered here.

As shown above, the use of a substrate with high trap and acceptor densities reduces the contribution of substrate conduction. It is also shown that using a thick p-buffer layer has the same effect as using a substrate with a high density of traps in the sense that both of them reduce the substrate current. It is demonstrated that when the p-buffer layer is fully depleted, the acceptors in the p-buffer layer play the same electrical role as the acceptors within the space-charge region of the semi-insulating substrate.

### C. Short-Channel Effects

The threshold voltage of a MESFET is an important parameter in GaAs IC's. Its shift with shortening the gate length is well known as the short-channel effect, and is fatal in circuit design. We discuss this phenomenon in terms of impurity densities in the p-buffer layer and in the semi-insulating substrate.

Fig. 11 shows an example of the $I_D$–$V_G$ characteristics of GaAs MESFET's without a p-buffer layer for different gate lengths. As the gate length becomes shorter, the $I_D$–$V_G$ curve shifts in the negative direction in $V_G$, and further, its gradient in the subthreshold region becomes smaller. This represents the short-channel effect. To repre-

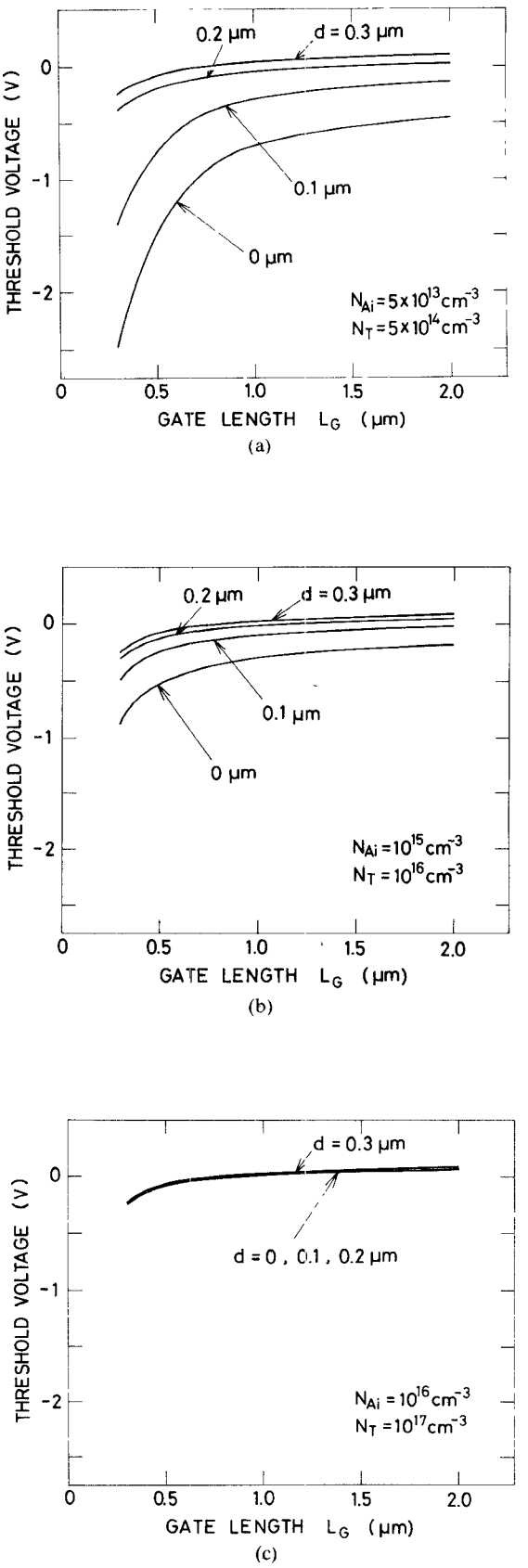


Fig. 12. Threshold voltage as a function of gate length for GaAs MESFET's on a p-buffer layer, with the thickness of a p-buffer layer, $d$, as a parameter. The threshold voltage is defined here as the gate voltage when $I_D$ becomes $5\times10^{-3}$ A/cm (5 μA/10 μm) at $V_D = 1$ V. Three cases with different trap and acceptor densities in the substrate are shown. (a) $N_{A_i} = 5\times10^{13}$ cm$^{-3}$, $N_T = 5\times10^{14}$ cm$^{-3}$. (b) $N_{A_i} = 10^{15}$ cm$^{-3}$, $N_T = 10^{16}$ cm$^{-3}$. (c) $N_{A_i} = 10^{16}$ cm$^{-3}$, $N_T = 10^{17}$ cm$^{-3}$.

sent the short-channel effects, we define the threshold voltage as the gate voltage when $I_D$ becomes $5\times10^{-3}$ A/cm (5 $\mu$A/10 $\mu$m) at $V_D=1$ V.

Fig. 12 shows the threshold voltage versus gate length with the thickness of a p-buffer layer, $d$, as a parameter. Three cases with different trap and acceptor densities in the substrate are shown. In the cases with relatively low trap and acceptor densities in the substrate (Fig. 12(a) and (b)), it is seen that for thinner $d$, the threshold voltage is more negative for a given gate length, and its shift with a shortening of the gate length is larger. The former can be understood by the fact that for thinner $d$, the effective channel becomes thicker because of the narrower space-charge region in the n layer, and also the potential barrier at the active layer–substrate interface is less steep. The latter arises from the increase in the direct substrate current with shortening of the gate length. This substrate current becomes important, as seen in Fig. 2 and Fig. 3, for shorter gate length MESFET's with thinner $d$. Therefore, the shift of the threshold voltage is pronounced in the case with thinner $d$. As is evident from Fig. 12, the short-channel effect is reduced when the trap and acceptor densities in the substrate are higher. It should be noted that in Fig. 12(c), the threshold voltage–gate length curves are almost independent of $d$. This is because in this case $N_{Ap}=N_{At}$ and so the negative charges in the substrate side are almost the same for all $d$ if the p-buffer layer is depleted. It is concluded that using a thick p-buffer layer has the same effect as using a substrate with a high density of traps since both of them lead to minimizing the short-channel effects in GaAs MESFET's.

As shown above, the substrate current must be decreased to minimize the short-channel effects. Qualitatively, it was shown by experiments [6] that using a buried p-layer or a p-buffer layer could reduce the short-channel effects. Quantitative comparison of the calculated results with experiments is an important work to be done in the future.

## IV. Conclusion

A numerical analysis of GaAs MESFET's with a p-buffer layer on the semi-insulating substrate is performed in which impurity compensation by traps in the substrate is considered. It is shown that the use of a thick p-buffer layer results in the lower device current due to the formation of a steep barrier at the channel–substrate interface. It is also shown that in a case with higher trap and acceptor densities in the substrate, the drain current becomes lower due to the decrease in the substrate current. This decrease in the substrate current occurs due to the formation of a negative space-charge layer in the substrate. It is demonstrated that when the p-buffer layer is fully depleted, the acceptors in the p-buffer layer play the same electrical role as the acceptors within the space-charge region of the semi-insulating substrate. It is concluded that using a thick p-buffer layer has the same effect as using a substrate with a high density of traps. Both of them lead to minimizing the short-channel effects in GaAs MESFET's. Therefore, even if the trap density in the substrate is low, the short-channel effects can be reduced by introducing a p-buffer layer or a buried p-layer.

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## References

[1] T Itoh and H. Yanai, "Stability of performance and interfacial problem in GaAs MESFET's," *IEEE Trans Electron Devices*, vol. ED-27, pp. 1037–1045, 1980.

[2] C Kocot and C A. Stolte, "Backgating in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol ED-29, pp. 1059–1064, 1982.

[3] S Makram-Ebeid and P. Minondo, "The roles of the surface and the bulk of the semi-insulating substrate in low-frequency anomalies of GaAs integrated circuits," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 632–642, 1985.

[4] G. M Martin, J P. Farges, G. Jacob, J. P. Hallaia, and G. Poiblaud, "Compensation mechanism in GaAs," *J Appl Phys.*, vol. 51, pp. 2840–2852, 1980

[5] K Horio, T Ikoma, and H. Yanai, "Computer-aided analysis of GaAs n-i-n structures with a heavily compensated i-layer," *IEEE Trans. Electron Devices*, vol. ED-33, pp 1242–1250, 1986.

[6] K. Yamasaki, N. Kato, and M. Hirayama, "Buried p-layer SAINT for very high-speed GaAs LSI's with submicrometer gate length," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 2420–2425, 1985.

[7] K Yamasaki, N. Kato, and M. Hirayama, "Below 10 ps/gate operation with buried p-layer SAINT FET's," *Electron Lett.*, vol. 20, pp. 1029–1031, 1984

[8] T Enoki, S Sugitani, K. Yamasaki, and K. Ohwada, "Reduction of the short-channel effects for GaAs MESFET's by double shallow $n^+$-layers," *IEEE Electron Device Lett.*, vol. EDL-9, pp. 470–472, 1988.

[9] K. Yamaguchi, S. Asai, and H. Kodera, "Two-dimensional numerical analysis of stability criteria of GaAs FET's," *IEEE Trans. Electron Devices*, vol ED-23, pp. 1283–1290, 1976.

[10] T. Wada and J. Frey, "Physical basis of short-channel MESFET operation," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 476–490, 1979.

[11] P Bonjour *et al*, "Saturation mechanism in 1 $\mu$m gate FET with channel-substrate interface barrier," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1019–1024, 1980

[12] A. Yoshii, M Tomizawa, and K. Yokoyama, "Accurate modeling for submicrometer-gate Si and GaAs MESFET's using two-dimensional particle simulation," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1376–1380, 1983.

[13] W. R. Curtice, "The performance of submicrometer gate length GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1693–1699, 1983.

[14] M. F. Absaid and J. R. Hauser, "A comparative analysis of GaAs and Si ion-implanted MESFET's," *IEEE Trans. Electron Devices*, vol. ED-33, pp 908–912, 1986.

[15] N. A.-Mishima and K. Yamaguchi, "A two-dimensional numerical analysis of GaAs MESFET's with a p-buffer layer," *Trans. IEICE*, vol. J70-C, pp. 631–636, 1987 (in Japanese).

[16] K. Horio, H. Yanai, and T. Ikoma, "Numerical simulation of GaAs MESFET's on the semi-insulating substrate compensated by deep traps," *IEEE Trans. Electron Devices*, vol. ED-35, pp. 1778–1785, 1988.

[17] K. Horio and H. Yanai, "Numerical analysis of GaAs MESFET's with p-buffer layer on semi-insulating substrate including deep traps," *Electron. Lett.*, vol. 25, pp 86–88, 1989.

[18] D E. Holmes, R. T. Chen, K R. Elliot, C. G Kirkpatrick, and P. W Yu, "Compensation mechanism in liquid encapsulated Czochralski GaAs: Importance of melt stoichiometry," *IEEE Trans Electron Devices*, vol. ED-29, pp. 1045–1051, 1982.

[19] D. L. Scharfetter and H. K. Gummel, "Large-signal analysis of a silicon Read diode oscillator," *IEEE Trans. Electron Devices*, vol. ED-16, pp 64–77, 1969

[20] H. K. Gummel, "Self-consistent iterative scheme for one-dimensional steady state transistor calculations," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 455–465, 1964.

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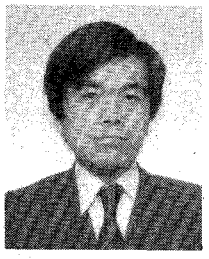

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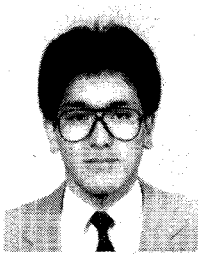

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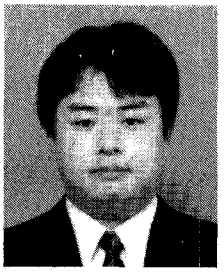

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